A Fully Differential 100 – 140 GHz Frequency Quadrupler in a 130 nm SiGe:C Technology for MIMO Radar Applications using the Bootstrapped Gilbert-Cell Doubler Topology

Simon Kueppers [1], Klaus Aufinger [2], Nils Pohl [3]
simon.kueppers@fhr.fraunhofer.de

[1]Fraunhofer Institute for High Frequency Physics and Radar Techniques,
Fraunhoferstr. 20, D-53343 Wachtberg, Germany
[2]Infineon Technologies AG, Am Campeon 1-12, D-85579 Neubiberg, Germany
[3]Ruhr-University Bochum, Universitaetsstr. 150, D-44801 Bochum, Germany

***Abstract*— This paper presents a frequency quadrupler implemented in a 130 nm SiGe:C technology suitable for radar systems with spatially distributed transmitters and receivers. The circuit is based on cascading the bootstrapped Gilbert-Cell doubler topology with differential inputs and differential outputs presented in [1]. In conjunction with a balancing input preamplifier and output buffer amplifier, a maximum power conversion gain of 26 dB and an output power of 0 – 4 dBm over 40 GHz (28 %) bandwidth in the range of 120 – 160 GHz is achieved. The frequency quadrupler operates at a power consumption of 132 mW with a 1 dB input gain compression point of −22 dBm. The differential output amplitude imbalance in the desired frequency range of 100 – 140 GHz is well below ±1 dB and the preamplifier input match is better than −10 dB between 25 – 35 GHz.**

***Index Terms*— radar, frequency doubler, gilbert-cell, SiGe, transformer, F-band**

I. Introduction

Large-scale multistatic radar applications such as MIMO based systems as described in [2] typically use a single reference source signal that is distributed to many spatially distributed receiver and transmitter circuits (see Fig. 1). However, the frequency range of the reference signal should be comparatively low such that dielectric, skin and radiation losses on coaxial or microstrip distribution networks can be reduced. Within the receiver and transmitter circuits, a coherent and low phase noise signal in the frequency range of the radar has to be generated from the distributed reference signal. For this purpose, several solutions such as phase-locked loops or injection locked oscillators could be used. Due to its robustness and feasibility for on-chip integration we focus on the use of a two-stage frequency quadrupler in order to generate a 100 – 140 GHz radar signal from a 25 – 35 GHz reference signal. The circuit building block presented in this paper will be the basis of the transmit (TX) and receive (RX) circuits shown in Fig. 1.

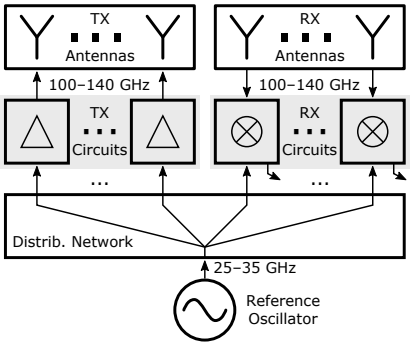

Fig. 1: System Concept of MIMO Radar System.

II. Circuit Architecture

The circuit architecture of the frequency quadrupler is shown in Fig. 2. In order to allow the distribution of a low-power reference signal to many transmitters and receivers, a high input sensitivity of the frequency quadrupler is desirable. Moreover, when the transmitters and receivers are distributed in electrically large systems, a good impedance match at the frequency quadrupler input is required in order to reduce multiple reflections of the reference signal along the distribution network. These reflections could otherwise produce unwanted frequency spurs at the output of the frequency quadrupler. While differential signaling is preferred in integrated circuits, the reference signal is realized as a single-ended transmission line to reduce routing and distribution effort to the spatially distributed receiver and transmitter nodes. In this work, a combination of a transformer-based balun and a differential high common-mode rejection common-base circuit has been used. The wideband input match has been realized by placing the transformer's secondary winding at the emitters of the transistors and applying a DC bias current of $I_c = V_T/(R_{in} - R_{em})$ where V_T is the thermal voltage, R_{in} the desired input resistance and R_{em} the intrinsic

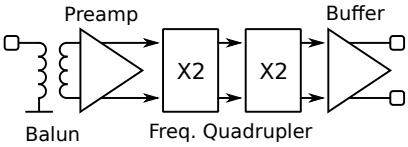

Fig. 2: Developed circuit architecture of the frequency quadrupler with preamp and output buffer.

emitter resistance.

In order to quadruple the input signal in frequency, several different circuit topologies have been reported in literature ([3], [4], [5], [6]). For driving the intended on-chip loads such as power amplifiers or receive mixers, a differential signal with moderate power is required. To satisfy the requirement, either fully differential frequency doubler circuits such as Gilbert-Cell doublers or single-ended output doublers such as push-push in combination with baluns are required. While Gilbert-Cell show similar amplitude and phase imbalance to push-push doublers with transformer or transmission line based baluns they are capable of providing a higher conversion gain at a lower power consumption ([7], [5]).

In recent publications, different methods of reducing the residual amplitude and phase imbalance have been presented. In [8] an additional common-mode suppressing transformer has been used. However, this circuit still suffers from losses in the transformer at the relevant frequency range resulting in a lower overall conversion gain.

Another approach for improving the quality of the output signal was presented in [2]. By modifying the conventional Gilbert-Cell topology (Fig. 3a) and introducing additional delay lines (see Fig. 3b), a high conversion gain can be achieved with a low amplitude and phase imbalance in a wide frequency range. This bootstrapped Gilbert-Cell

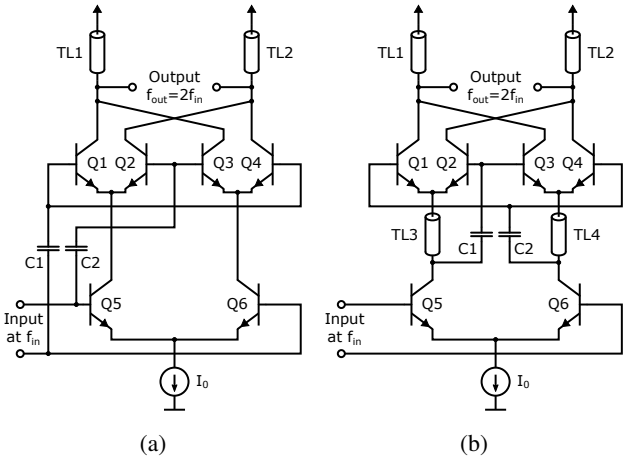

Fig. 3: Comparison of conventional Gilbert-Cell doubler (a) and bootstrapped Gilbert-Cell doubler (b) used in this paper.

topology has been used to develop the circuit architecture for the intended application as shown in Fig. 2. However due to the large $\lambda/4$ length of the transmission lines *TL3* and *TL4* at the center input frequency of 30 GHz in the first frequency doubler, inductors have been used instead.

To provide sufficient output power to drive onchip loads such as power amplifiers or mixer LO inputs, a buffer amplifier has been implemented. Additionally, the amplifier isolates the last doubler stage from loadpulling effects of an improperly matched output load and further improves any residual amplitude imbalance of the quadrupler core by employing a cascode amplifier with a tail current source and a high common-mode impedance of the cascode base node.

III. Implementation and Measurement Results

The circuit has been simulated and layouted in Infineon's B11HFC 130 nm SiGe:C BiCMOS technology featuring heterojounction bipolar transistors (f_T 250 GHz, f_{max} 370 GHz), RF capacitors and resistors, a metal stack of 6 copper layers and a top aluminium layer. The transformer used in the input preamplifier stage has been designed with the Keysight ADS Momentum EM solver and optimized using a parametrized model. Fig. 4 shows a photograph of the frequency quadrupler circuit with an overall size of 770 µm × 220 µm.

The circuit operates at 40 mA with a supply voltage of 3.3 V, resulting in a total power consumption of 132 mW (preamplifier 32 mW, frequency doublers 32 mW and 38 mW, buffer amplifier 30 mW). The frequency response of the circuit (Fig. 5) shows a peak output power of more than 4 dBm at 142 GHz. The shift in frequency is due to the interaction of the parasitic output network (dashed in Fig. 4) and the load lines of the output buffer amplifier. The network will not be present, when the circuit is being operated with well matched on-chip loads as intended. The output half-power bandwidth is about 28 GHz between 128 – 156 GHz. The total available power has been calculated as the sum of the single-ended output signals in consecutive measurements thus neglecting any residual phase difference at the output. The ripple shown in the

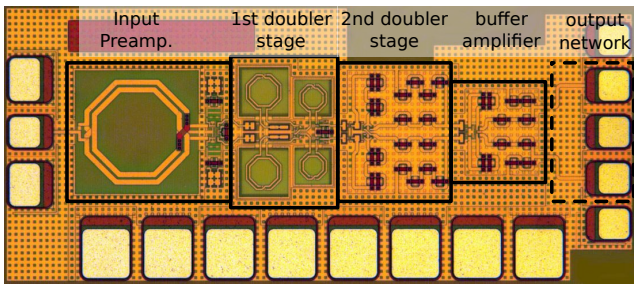

Fig. 4: Chip photograph of the circuit architecture shown in Fig. 2.

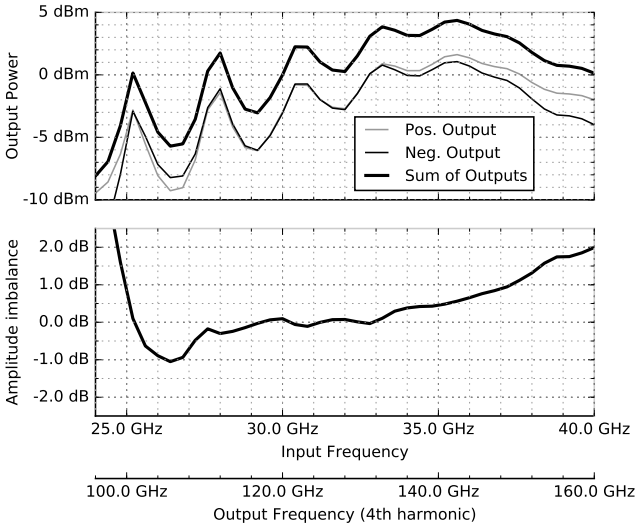

Fig. 5: Measurement of output power (top) and amplitude imbalance (bot.) of single-ended outputs ($P_{in} = -15\,\mathrm{dBm}$)

output power curve is due to the WR-6 waveguide probe used in the measurement setup. The output power has been measured with an Erickson PM4 calorimeter and has been corrected by the losses in the measurement setup. The bottom curve in Fig. 5 shows the amplitude imbalance of the single-ended outputs which is well below ± 1 dB in the original target frequency range of 100 – 140 GHz.

Fig. 6 shows that the input match of the input preamplifier is below −10 dB in the frequency range of 20 – 40 GHz between 25 °C and 75 °C improving to −15 dB between 25 – 35 GHz in conjunction with a typical 100 pH bondwire. In Fig. 7, the maximum power conversion gain is 26 dB and the input referred 1 dB gain compression point is −22 dBm.

IV. Conclusion

In this paper, a circuit suitable for the generation of a local oscillator signal in spatially distributed radar systems is presented. The novel bootstrapped Gilbert-Cell architecture from [1] has been implemented in a 130 nm SiGe:C technology and characterized. A maximum output power of more than 4 dBm is achieved at a power conversion gain

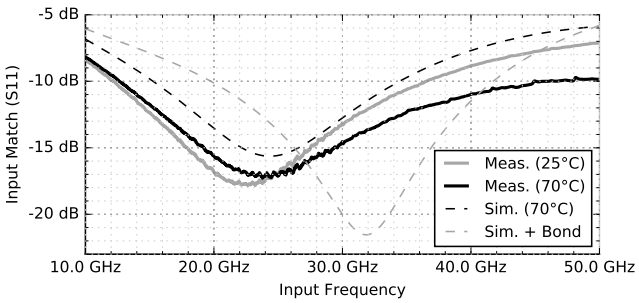

Fig. 6: Measurement and simulation of preamplifier input match at different temperatures.

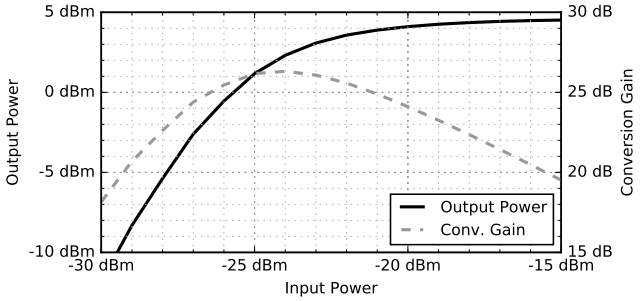

Fig. 7: Measurement of power and gain compression at 142 GHz.

of 24 dB. The total power consumption is 132 mW and a minimum input power of −20 dBm is required for the output power to saturate at 4 dBm. To the authors knowledge the combination of these numbers are unmatched by current literature in the frequency range of 120 – 160 GHz. The reference signal input match is below −10 dB between 25 – 35 GHz which is sufficient to avoid frequency spurs at the output of the frequency quadrupler. The work shown in this paper will be a suitable basis for future transmit and receive circuits in a MIMO radar system.

Acknowledgment

This work has partly been supported within H2020-ICT by the European Commission under grant agreement number 645101 (SmokeBot). We would also kindly like to thank Infineon Technologies AG for the production of the integrated circuits.

References

[1] S. Yuan and H. Schumacher, "90-140 GHz frequency octupler in Si/SiGe BiCMOS using a novel bootstrapped doubler topology," in *European Microwave Integrated Circuit Conference (EuMIC), 2014 9th*, Oct 2014, pp. 158–161.

[2] S. S. Ahmed, A. Schiessl, and L. P. Schmidt, "A Novel Fully Electronic Active Real-Time Imager Based on a Planar Multistatic Sparse Array," *IEEE Transactions on Microwave Theory and Techniques*, vol. 59, no. 12, pp. 3567–3576, Dec 2011.

[3] Y. Sun and C. J. Scheytt, "An integrated harmonic transmitter front-end for 122 GHz FMCW/CW radar sensor," in *Microwave Integrated Circuits Conference (EuMIC), 2011 European*, Oct 2011, pp. 97–100.

[4] R. B. Yishay and D. Elad, "A 17.8 dBm 110-130 GHz Power Amplifier and doubler chain in SiGe BiCMOS technology," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2015 IEEE*, May 2015, pp. 391–394.

[5] V. Valenta, S. Yuan, A. Trasser, and H. Schumacher, "F-band frequency octupler in 0.13um SiGe:C BiCMOS with 2 mW output power," in *Microwave Symposium Digest (IMS), 2013 IEEE MTT-S International*, June 2013, pp. 1–3.

[6] C. Bredendiek, N. Pohl, K. Aufinger, and A. Bilgic, "An ultra-wideband D-Band signal source chip using a fundamental VCO with frequency doubler in a SiGe bipolar technology," in *2012 IEEE Radio Frequency Integrated Circuits Symposium*, June 2012, pp. 83–86.

[7] S. Yuan and H. Schumacher, "A SiGe:C BiCMOS 140 GHz wideband frequency multiplier-by-8 with differential output," in *Microwave Integrated Circuits Conference (EuMIC), 2013 European*, Oct 2013, pp. 248–251.

[8] S. Yuan and H. Schumacher, "Compact V band frequency doubler with true balanced differential output," in *2013 IEEE Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, Sept 2013, pp. 191–194.